REMARKS

The 05 June 2002 official action addressed claims 21-26. Claims 21, 24 and 26 have been amended. Claim 25 has been canceled without prejudice. No new matter has been added. Thus, claims 21-24 and 26 are present for examination.

Claims 21-26 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The rejection is respectfully traversed.

In paragraph 2 of the instant official action, the Examiner states that it is not clear in the originally filed specification "where support for 'each word line having a plurality of . . . floating gates' can be found."

Claims 21 and 24 have been amended to recite a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising, *inter alia* :

" . . . patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon strips to thereby form a plurality of control gates and a plurality of floating gates, said plurality of control gates serving as a plurality of word lines . . .".

Support for this amendment may be found in Applicants' specification at, *inter alia*, page 12, lines 20-27. Thus, Applicants believe that claims 22-24 and 26 now fully comply with 35 U.S.C. 112, first paragraph.

Claims 21-26 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

The rejection is respectfully traversed.

In paragraph 3 of the instant official action, the Examiner states that "[i]t is not clear how, if the control gate and the word lines are the same thing as was originally disclosed, the plurality of field insulating films can be parallel to something at the time of its formation that has not yet been formed." In paragraph 5, the Examiner questions how a plurality of field insulating films and first polysilicon strips can be perpendicular to "later formed" word lines.

Claims 21 and 24 have been amended to recite a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising, *inter alia*:

"(a) forming a plurality of field insulating films in parallel with one another;

. . .

(c) forming a plurality of first polysilicon strips in parallel with one another;

. . .

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon strips to thereby form a plurality of control gates and a plurality of floating gates, said plurality of control gates serving as a plurality of word lines, said plurality of word lines being perpendicular to said plurality of field insulating films and said plurality of first polysilicon strips;

. . . ."

Applicants believe that claims 21 and 24 now clearly recite the claimed subject matter, support for which may be found in Applicants' specification at, *inter alia*, page 13, line 5 through page 14, line 28. Thus, Applicants believe that claims 22-24 and 26 now fully comply with 35 U.S.C. 112, second paragraph.

In paragraph 6, the Examiner rejects claims 21-26 under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements by defining a position of a feature of an invention in respect to a position of a different feature that has not yet been formed.

Applicants believe that, as a result of the amendment to claims 21 and 24 discussed above, claims 22-24 and 26 now fully comply with 35 U.S.C. 112, second paragraph.

In paragraph 7 of the instant official action, claims 21, 22, and 24 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, et al. (U.S. Patent No. 5,838,615) (hereinafter "Kamiya") in view of Nishihara (JP 08204159) (hereinafter "Nishihara") and Kim (U.S. Patent No. 5,834,807) (hereinafter "Kim").

The rejection is respectfully traversed.

Claim 21, as amended, recites a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors wherein

". . .

said first metal wiring layer completely filling said contact-holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact-holes,

said first metal wiring layer extends in parallel with said plurality of field insulating films and offset from said plurality of field insulating films such that said first metal wiring layer does not make contact with said plurality of field insulating films, and

said first metal wiring layer forms a continuous portion connecting ones of said plurality of contact-holes formed above said source regions, and forms isolated island regions above ones of said plurality of contact-holes formed above said drain regions."

Neither Kimaya, Nishihara nor Kim disclose or suggest the claimed invention, including the above-quoted features.

As best shown in FIGS. 11D and 13, Applicants' first metal wiring layer 12a, 12b, 12c, 12d completely fills the contact-holes 11 formed above drain and source regions 8a, 8b. Portions of the first metal wiring layer 12c, 12d have a width wider than a diameter of the contact-holes 11.

As best shown in FIGS. 14 and 15, Applicants' first metal wiring layer 12c, 12d extends in parallel with the field insulating films 3 offset from the field insulating films 3 such that the first metal wiring layer 12c, 12d does not make contact with the field insulating films 3.

As best shown in FIG. 9, Applicants' first metal wiring layer 12a, 12b is forms a continuous portion 12a connecting ones of said plurality of contact-holes 11 formed above said source regions 8b, and forms isolated island regions 12b above ones of said plurality of contact-holes 11 formed above said drain regions 8a.

Because neither Kimaya, Nishihara nor Kim, alone or in combination, disclose or suggest the claimed invention, including the above-quoted features, the subject matter of Applicants' invention as a whole would not have been obvious at the time the invention was made to a person having ordinary skill in the art. Thus, the Patent and Trademark Office has not made out a prima facie case of obviousness under the provisions of 35 U.S.C. 103(a) and claim 21, as amended, is believed to be allowable.

Claims 22 and 23 depend directly from amended claim 21 and are, for at least this reason, believed to be allowable.

Claim 24, as amended, recites a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising, *inter alia*:

". . .

(k) forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line,

. . .

said first metal wiring layer completely filling said contact-holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact-holes,

said first metal wiring layer extends in parallel with said plurality of field insulating films and offset from said plurality of field insulating films such that said first metal wiring layer does not make contact with said plurality of field insulating films, and

said first metal wiring layer forms a continuous portion connecting ones of said plurality of contact-holes formed above said source regions, and forms isolated island regions above ones of said plurality of contact-holes formed above said drain regions."

Neither Kimaya, Nishihara nor Kim disclose or suggest the claimed invention, including the above-quoted features.

Claim 24, as amended, recites the same patentably distinct features as recited in amended claim 21 discussed above. Thus, for at least the same reasons discussed above in relation to claim 21, claim 24, as amended, is believed to be allowable.

In addition, claim 24 recites "forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line".

In paragraph 10 of the instant official action, the Examiner recognizes that neither Kimaya, Nishihara nor Kim disclose forming backing wiring layers. Accordingly, the Examiner cited Cacharelis et al. (U.S. Patent No. 5,550,072) (hereinafter "Cacharelis") with respect to that feature.

Cacharelis teaches that "a second metal layer 500 is deposited and patterned on the surface of second dielectric layer 480. As is evident in FIG. 21A, the patterning of metal layer 500 forms a word line 500W which extends perpendicular to bit line 470B. By means of vias 440 and 490 and tab 440T, word line 500W connects to the control gate of memory transistor 2." (See col. 5, lines 47-54.) However, Cacharelis does not teach or

suggest "forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line", as recited in Applicants' amended claim 24.

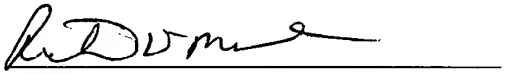
Accordingly, even if Cacharelis could be combined with Kimaya, Nishihara and/or Kim as suggested by the Examiner, the combination would not meet the claimed invention. Thus, the Patent and Trademark Office has not made out a prima facie case of obviousness under the provisions of 35 U.S.C. 103(a) and, for this additional reason, claim 24, as amended, is believed to be allowable.

Claim 26 has been amended to change its dependency from cancelled claim 25 to claim 24. Thus, claim 26 now depends directly from amended claim 24 and is, for at least this reason, believed to be allowable.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Reexamination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

Date: December 4, 2002



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Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 19-0741 for any such fees; and applicant(s) hereby petition for any needed extension of time.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Takaaki NAGAI et al.

Title: EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Appl. No.: 09/606,159

Filing Date: 06/29/2000

Examiner: P. Brock, II

Art Unit: 2815

MARKED-UP VERSION OF AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed June 5, 2001, time for response to which is extended three months (to December 5, 2002) by the accompanying petition, please amend the above-identified application as follows:

IN THE CLAIMS:

Please enter the following amended claims:

21. (Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another ~~and perpendicular to a later formed plurality of word lines~~ on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon strips in parallel with one another ~~perpendicularly to said plurality of word lines~~;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon strips to thereby form ~~said~~ a plurality of control gates and a plurality of floating gates, said plurality of control gates serving as a plurality of word lines, ~~each~~ said plurality of word lines ~~having a plurality of control gates and floating gates~~being perpendicular to said plurality of field insulating films and said plurality of first polysilicon strips;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said plurality of word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said plurality of word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,

wherein said bottom portion of said bit line is connected to a top portion of said plurality of bit studs and a bottom portion of said plurality of bit studs is connected to said drain regions~~.~~,

said first metal wiring layer fills therewith all of said contact-holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact-holes,

said first metal wiring layer extends in parallel with said plurality of field insulating films above said plurality of film insulating films with respect to a distance from said

semiconductor substrate such that said first metal wiring layer does not make contact with said plurality of field insulating films, and

said first metal wiring layer is formed with a raised portion only above ones of said plurality of contact-holes formed above said source regions, and is formed in an island shape above ones of said plurality of contact-holes formed above said drain regions.

22. The method as set forth in claim 21, wherein said second gate insulating film has a three-layered structure of oxide/nitride/oxide films.

23. The method as set forth in claim 21, wherein said first and second metal wiring layers are composed of aluminum.

24. (Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another ~~and perpendicular to a later formed plurality of word lines~~ on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon strips in parallel with one another ~~perpendicularly to said plurality of word lines~~;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon strips to thereby form ~~said~~ a plurality of control gates and a plurality of floating gates, said plurality of control gates serving as a plurality of word lines, ~~each~~ said plurality of word lines ~~having a plurality of control gates and floating gates~~being perpendicular to said plurality of field insulating films and said plurality of first polysilicon strips;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said plurality of word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); ~~and~~

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line~~,~~; and

(k) forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line,

wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions~~.~~,

said first metal wiring layer fills therewith all of said contact-holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact-holes,

said first metal wiring layer extends in parallel with said plurality of field insulating films above said plurality of film insulating films with respect to a distance from said semiconductor substrate such that said first metal wiring layer does not make contact with said plurality of field insulating films, and

said first metal wiring layer is formed with a raised portion only above ones of said plurality of contact-holes formed above said source regions, and is formed in an island shape above ones of said plurality of contact-holes formed above said drain regions.

Please cancel claim 25.

26. (Amended) The method as set forth in claim ~~25~~24, wherein said backing wiring layers are constituted of said second metal wiring layer.